FORM PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
162.7106USU	10/896,071
Applicant: Bhattacharya et al.	
Filing Date: June 29, 200	Group Art Unit: 2811

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (including Author, Title, Date, Pertinent Pages, Etc.)

TD	Kazuo Taki, "*A Survey for Pass-Transistor Logic Technologies*", IEEE, 1998.
TD	Mineo Kaneko and Jialin Tian, "*Concurrent Cell Generation and Mapping for CMOS Logic Circuits*", IEEE, 1997.
TD	C. P. Liu and J. A. Abraham, "*Transistor Level synthesis for Static CMOS Combinational Circuits*", Proc. 9th Great Lake Symposium on VLSI, pp. 172-175, 1999.

EXAMINER	DATE CONSIDERED
Ulwando	6/12/03

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Sheet 1 of 1.

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TD	S. Gavrilov, A. Glebov, "*Library-Less Synthesis for Static CMOS Combinational Logic Circuits*", Research Institute for BLSI CAD Systems, Russian Academy of Science, IEEE 1997.
TD	C. Yang and M. Ciesielski, "*Synthesis for Mixed CMOS/PTL Logic: Preliminary Results*", Department of Electrical and Compute Engineering, University of Massachusetts.

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